

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A tool for use in a process related to testing a circuit device, comprising:
code for identifying a respective parent portion and any respective branch portions of a scan chain of a circuit device, the scan chain having a scan input and one or more scan outputs and a plurality of scan cells disposed therebetween; and

code for creating a model of the scan chain, including code for creating a dummy cell chain which includes creating one or more dummy cells and connecting the one or more dummy cells between the scan input and a branch portion of the scan chain.

Claim 2 (original): A tool as in claim 1, wherein the process related to testing a circuit device is a process selected from the group consisting of: creating a test, generating a test pattern, automatically generating a test pattern, validating a test, verifying a test, setting up a test or running a test.

Claim 3 (original): A tool according to claim 1 wherein the code for creating a dummy cell chain further includes code selected from the group consisting of:

code for breaking the branch portion from the parent portion of the scan chain in the model;

code for inserting the one or more dummy cells in the branch chain immediately prior to the existing cells in the branch chain and immediately after the scan input;

code for creating the dummy chain in parallel to the parent chain; and

code for creating exactly the same number of dummy cells exactly matching the number of non-branched parent cells in the parent portion of the scan chain.

Claim 4 (original): A tool as in claim 1, further including code for preliminarily determining whether the scan chain has a plurality of outputs.

Claim 5 (original): A tool as in claim 1, further including code selected from the group of code for determining whether there remain any branch portions of the scan chain for which a dummy cell chain may be created; and code for determining whether there remain any branch portions off another branch portion of the scan chain for which a dummy cell chain may be created.

Claim 6 (original): A tool as in claim 1, wherein the tool is at least part of a computer program and the code portions thereof are program codes.

Claim 7 (original): A tool as in claim 1, wherein the tool is at least partly comprised of hardware.

Claim 8 (original): A tool as in claim 1, wherein the circuit device is selected from the group consisting of an IC device and a circuit board.

Claim 9 (original): A tool as in claim 1, wherein the model is communicated to circuit test equipment for use during testing of the circuit device.

Claim 10 (original): A tool as in claim 1, wherein the tool is adapted to communicate with apparatus selected from the group consisting of: test equipment; or automated test equipment; or computer equipment for test pattern generation or validation.

Claim 11 (original): A tool as in claim 1, wherein the tool forms a part of apparatus selected from the group consisting of: test equipment; or automated test equipment; or computer equipment for test pattern generation or validation.

Claim 12 (original): A tool as in claim 1, wherein the tool provides an abstract software model of the circuit device to apparatus selected from the group consisting of: test equipment, automated test equipment and computer equipment for test pattern generation or validation.

Claim 13 (currently amended): A tool for use in a test process for a device, comprising:
means for identifying respective parent and branch portions of a scan chain of the device;
and
means for creating [[an]] a model of the scan chain, including:
means for breaking the branch portion from the parent portion of the scan chain in
the model;
means for inserting one or more dummy cells in the branch chain prior to the
existing cells in the branch chain; and
means for re-connecting the branch chain with the inserted dummy cells to the
scan input in the model of the scan chain.

Claim 14 (currently amended): A tool for use in a test process for a circuit device comprising:
an electronic representation of a branched scan chain of the circuit device, the branched
scan chain having scan cells in a parent portion and a branched portion, the branched portion
branching off the parent portion;
whereby the electronic representation includes:
a representative parent portion of scan cells; [[.]] and
a branched dummy portion of scan cells; [[.]]
whereby the representative parent portion is an electronic representative of the scan cells
of the parent portion of the branched scan chain of the circuit device; [[.]] and
whereby the branched dummy portion includes:
an electronic representative of the scan cells of the branched portion of the
branched scan chain of the circuit device; and
one or more dummy scan cells disposed prior to the electronic representative scan
cells of the branched portion of the branched scan chain, and whereby the dummy scan cells are
connected to the electronic representative of the scan cells of the branched portion of the
branched scan chain, such that the dummy scan cells are disposed to communicate therewith.

Claim 15 (original): A tool as in claim 14, wherein the tool is an abstract software model of the
circuit device used with apparatus selected from the group consisting: of test equipment;
automated test equipment; and computer equipment for test pattern generation or validation.

Claim 16 (currently amended): A system for setting up a test for a circuit device comprising:
a test pattern generator which receives input relative to a circuit device to be tested and which outputs a test pattern for testing the circuit device;
a tool which operates with the test pattern generator, the tool having:
means for identifying respective parent and branch portions of a scan chain of a circuit device, the scan chain having a scan input and a plurality of scan outputs and a plurality of scan cells; and
means for creating [[an]] a model of the scan chain, including means for creating a dummy cell chain which includes the branch portion of the scan chain connected with one or more dummy cells and the scan input.

Claim 17 (original): A method for modeling test circuitry of a device comprising:
identifying respective parent and branch portions of a scan chain of the device, the scan chain having a plurality of scan cells and at least one scan input and a plurality of scan outputs;
and
creating a model of the scan chain, the model comprising the parent portion of the scan chain, and dummy cells connected between the scan input and the branch portion of the scan chain.

Claim 18 (original): A method as in claim 17, wherein said creating a model further comprises:
disconnecting the branch from the parent.

Claim 19 (original): A method for performing a test-related process for a circuit device comprising:
identifying respective parent and branch portions of an actual scan chain of a circuit device, the actual scan chain having a plurality of scan cells and at least one scan input and a plurality of scan outputs; and
creating a model of the scan chain, including creating a dummy cell chain which includes the branch portion of the scan chain connected with one or more dummy cells and the scan input.

Claim 20 (original): A method as in claim 19, wherein the test-related process is a process selected from the group consisting of: creating a test, generating a test pattern, automatically generating a test pattern, validating a test, verifying a test, setting up a test or running a test.

Claim 21 (currently amended): A method for testing a circuit device comprising:
using [[an]] a model of a scan chain of a circuit device, including a parent portion and a dummy cell portion of the representative chain, the dummy cell portion including the branch portion of the scan chain connected with one or more dummy cells and a common scan input which is in common with the parent portion;
shifting test bits into a common scan input;
populating the parent and the dummy portions of the model which includes populating the branch portion of the scan chain; and
capturing a response to the test bits shifted into the scan input.